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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/940,324	08/27/2001	Robert T. George	2207/12003	5090

25693 7590 04/20/2005

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EXAMINER	
KIM, HONG CHONG	
ART UNIT	**PAPER NUMBER**
2186	

DATE MAILED: 04/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/940,324	GEORGE ET AL.	
	Examiner	Art Unit	
	Hong C Kim	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

1. Claims 1-17 are presented for examination. This office action is in response to the amendment filed on 2/7/05.

2. The examiner requests, in response to this Office action, any reference(s) known to qualify as prior art under 35 U.S.C. sections 102 or 103 with respect to the invention as defined by the independent and dependent claims. That is, any prior art (including any products for sale) similar to the claimed invention that could reasonably be used in a 102 or 103 rejection. This request does not require applicant to perform a search. This **request** is not intended to interfere with or go beyond that **required** under 37 C.F.R. 1.56 or 1.105.

The request may be fulfilled by asking the attorney(s) of record handling prosecution and the inventor(s)/assignee for references qualifying as prior art. A simple statement that the query has been made and no prior art found is sufficient to fulfill the request. Otherwise, the fee and certification requirements of 37 CFR section 1.97 are waived for those documents submitted in reply to this request. This waiver extends only to those documents within the scope of this request that are included in the application's first complete communication responding to this requirement. Any supplemental replies subsequent to the first communication responding to this request and any information disclosures beyond the scope of this are subject to the fee and certification requirements of 37 CFR section 1.97.

In the event prior art documentation is submitted, a discussion of relevant

passages, figs. etc. with respect to the claims is requested. The examiner is looking for specific references to 102/103 prior art that identify independent and dependent claim limitations. Since applicant is most knowledgeable of the present invention and submitted art, his/her discussion of the reference(s) with respect to the instant claims is essential. **A response to this inquiry is greatly appreciated.**

The examiner also requests, in response to this Office action, support be shown for language added to any original claims on amendment and any new claims. That is, indicate support for newly added claim language by specifically pointing to page(s) and line number(s), in the specification and/or drawing figure(s). This will assist the examiner in prosecuting the application.

DOUBLE-PATENTING

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double

patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claims 1-17 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-30 of copending application No. 10/231,414. Claims of copending application No. 10/231,414 contains every element of claims 1-17 of the instant application and as such anticipates claims 1-17 of the instant application.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-4, 6-12, and 14 are rejected under 35 U.S.C. 102(e) s being anticipated by Chiu et al. (Chiu) U.S. Patent Application 2002/01994429.

As to claim 1, Chiu discloses the invention as claimed. Chiu discloses a cache-coherent I/O device (Fig. 1) comprising: a plurality of client ports (Fig. 1 Refs. 106's and 108's), each to be coupled to one of a plurality of port components (Fig. 1 Refs. 110's); a plurality of sub-unit caches (Fig. 1 Refs. 114), each coupled to one of said plurality of client ports and assigned to one of said plurality of port components; and a coherency engine (block 37) coupled to said plurality of sub-unit caches.

As to claim 2, Chiu discloses the invention as claimed in the above. Chiu further discloses wherein said plurality of port components includes processor port components (Fig. 1 Ref. 110, each disk is coupled to Host 102).

As to claim 3, Chiu discloses the invention as claimed in the above. Chiu further discloses wherein said plurality of port components includes input/output components (Fig. 1 Ref. 110, each disk is capable of I/O).

As to claim 4, Chiu discloses the invention as claimed in the above. Chiu further discloses wherein said plurality of sub-unit caches includes transaction buffers using a coherency logic protocol (block 54, free, shared or exclusive).

As to claim 6, Chiu discloses the invention as claimed. Chiu discloses a cache-processing system comprising (Fig. 1): a processor (Fig. 1 Ref 102); a plurality of port components (Fig. 1 Refs. 110's); and a cache-coherent I/O device (Fig. 1 Ref. 110 and block 37) coupled to said processor and including a plurality of client ports (Fig. 1 Refs. 106 and 108), each coupled to one of said plurality of port components (Fig. 1 Refs. 110's), said cache-coherent device further including a plurality of caches (Fig. 1 Refs. 114's), each coupled to one of said plurality of client ports and assigned to one of said plurality of port components, and a coherency engine (block 37) coupled to said plurality of caches.

As to claim 7, Chiu discloses the invention as claimed in the above. Chiu further discloses wherein said plurality of port components includes processor port components (Fig. 1 Refs. 110's).

As to claim 8, Chiu discloses the invention as claimed in the above. Chiu further discloses wherein said plurality of port components includes input/output components (Fig. 1 Refs. 110's).

As to claim 9, Chiu discloses the invention as claimed. Chiu discloses in a cache-coherent I/O device (Fig. 1) including a coherency engine (block 37) and a plurality of client ports (Fig. 1 Refs 106 and 108), a method for processing a transaction, comprising: receiving a transaction request (block 47, receiving a request to write data)

at one of said plurality of client ports on the I/O cache-coherent device, said transaction request includes an address (block 47, track); and determining whether said address is present (block 47, cache 114 hit) in one of a plurality of sub-unit caches (Fig. 1 Refs. 114), each of said sub-unit caches assigned to said one of said plurality of client ports (block 47, assign the relevant track to the allocated cache).

As to claim 10, Chiu discloses the invention as claimed in the above. Chiu further discloses wherein said transaction request is a read transaction request (block 54).

As to claim 11, Chiu discloses the invention as claimed in the above. Chiu further discloses transmitting data for said read transaction request from said one of said plurality of sub-unit caches to one of said plurality of client ports (block 54, determination is made regarding whether or not the data is in the local cache).

As to claim 12, Chiu discloses the invention as claimed in the above. Chiu further discloses prefetching one or more cache lines ahead of said read transaction request (cache memory reads on this limitation since the cache memory is used to assure that the currently useful data of main memory are copied into the small and fast cache for the purpose of increasing data access speed by means of spatial and temporal localities); and updating the coherency state (block 54, free, shared or exclusive) information in said plurality of sub-unit caches.

As to claim 14, Chiu discloses the invention as claimed in the above. Chiu further discloses wherein said transaction request is a write transaction request (block 47).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 5, 13, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiu et al. (Chiu) U.S. Patent Application 2002/01994429 in view of Jim Handy, "The Cache Memory Handbook" TK7895.M4H35, 1993, pp 140-240.

As to claims 5 and 13, Chiu discloses the invention as claimed above. However, Chiu dos not specifically disclose wherein said coherency logic protocol includes a Modified-Exclusive-Shared-Invalid (MESI) cache coherency protocol.

However, it is well known in the cache art to using MESI cache coherency protocol for the purpose of maintaining data consistency thereby increasing the memory access speed. For example, Handy discloses coherency logic protocol includes a Modified-Exclusive-Shared-Invalid (MESI) cache coherency protocol (Page 159).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to add coherency logic protocol includes a Modified-Exclusive-Shared-Invalid (MESI) cache coherency protocol of Handy into the invention of Chiu for the advantages stated above.

As to claim 15, Chiu and Handy disclose the invention as claimed in the above. Handy further discloses modifying coherency state information for a cache line in said one of said plurality of sub-unit caches; updating coherency state information in others of said plurality of sub-unit caches by said coherency engine; and transmitting data for said write transaction request from said one of said plurality of sub-unit caches to memory (MESI protocol reads on this limitation and pages 159-161).

7. Claims 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiu et al. (Chiu) U.S. Patent Application 2002/01994429 in view of Jim Handy, "The Cache Memory Handbook" TK7895.M4H35, 1993, pp 140-240 and further in view of Witt et al. (Witt) U.S. Patent 6,202,139.

As to claim 16, Chiu further discloses modifying coherency state information of said write transaction request (block 47), however, neither Chiu nor Handy specifically discloses write transaction request in the order received and pipelining multiple write requests.

Witt discloses write transaction request in the order received and pipelining multiple write requests (col. 2 lines 42-43) for the purpose of avoiding bank conflicts

thereby decreasing the performance losses and increasing the access speed (col. 2 lines 43-45).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate write transaction request in the order received and pipelining multiple write requests as shown in Witt into the combined invention of Chiu and Handy because it would avoid bank conflicts thereby decreasing the performance losses and increasing the access speed.

As to claim 17, Chiu, Handy and Witt disclose the invention as claimed in the above. Handy further discloses wherein the coherency state information includes a Modified-Exclusive-Shared-Invalid (MESI) cache coherency protocol (Page 159).

8. Alternatively, Claims 1-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. (Lee) U.S. Patent 6,477,621 in view of Jim Handy, "The Cache Memory Handbook" TK7895.M4H35, 1993, pp 140-240.

As to claim 1, Lee discloses a cache-coherent I/O device (Fig. 3) comprising: a plurality of client ports (Fig. 3 Refs. 501-507), each to be coupled to one of a plurality of port components (Fig. 3 Refs. 401-404); a plurality of sub-unit caches (Fig. 2 Refs. 601-607), each coupled to one of said plurality of client ports and assigned to one of said plurality of port components, however, Lee does not specifically disclose a coherency engine coupled to said plurality of sub-unit caches.

However, it is well known in the cache art to using a coherency engine for the purpose of maintaining data consistency thereby increasing the memory access speed. For example, Handy discloses a coherency engine (Page 159).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to add a coherency engine of Handy into the invention of Lee for the advantages stated above.

As to claim 2, Lee and Handy disclose the invention as claimed in the above. Lee further discloses wherein said plurality of port components includes processor port components (Fig. 3 Refs. 401-404, each mem bank is coupled to processor).

As to claim 3, Lee and Handy disclose the invention as claimed in the above. Lee further discloses wherein said plurality of port components includes input/output components (Fig. 3 Refs. 401-404, each mem bank is capable of I/O).

As to claim 4, Lee and Handy disclose the invention as claimed in the above. Handy further discloses wherein said plurality of sub-unit caches includes transaction buffers using a coherency logic protocol (sections 4.2.5, processor bits and 4.3.1, MESI).

As to claim 13, Lee and Handy disclose the invention as claimed above. Handy further disclose wherein said coherency logic protocol includes a Modified-Exclusive-Shared-Invalid (MESI) cache coherency protocol (Page 159).

As to claim 6, Lee discloses a cache-processing system comprising (Fig. 3): a processor (col. 5 lines 23-24); a plurality of port components (Fig. 3 Refs. 401-404); and a cache-coherent I/O device (Fig. 3 Refs. 601-607) coupled to said processor and including a plurality of client ports (Fig. 3 Refs. 501-507), each coupled to one of said plurality of port components, said cache-coherent device further including a plurality of caches (Fig. 3 Refs. 601-607), each coupled to one of said plurality of client ports and assigned to one of said plurality of port components, however, Lee does not specifically disclose a coherency engine coupled to said plurality of sub-unit caches.

However, it is well known in the cache art to using a coherency engine for the purpose of maintaining data consistency thereby increasing the memory access speed. For example, Handy discloses a coherency engine (Page 159).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to add a coherency engine of Handy into the invention of Lee for the advantages stated above.

As to claim 7, Lee and Handy disclose the invention as claimed in the above. Lee further discloses wherein said plurality of port components includes processor port components (Fig. 3 Refs. 401-404).

As to claim 8, Lee and Handy disclose the invention as claimed in the above. Lee further discloses wherein said plurality of port components includes input/output components (Fig. 3 Refs. 401-404).

As to claim 9, Lee discloses in a cache-coherent I/O device (Fig. 3) including a plurality of client ports (Fig. 3 Refs 501-507), a method for processing a transaction, comprising: receiving a transaction request (col. 5 lines 50-51) at one of said plurality of client ports on the I/O cache-coherent device, said transaction request includes an address (col. 10 lines 9-20); and determining whether said address is present (col. 10 lines 17-20) in one of a plurality of sub-unit caches (Fig. 3 Refs. 601-607), each of said sub-unit caches assigned to said one of said plurality of client ports (col. 10 lines 23-28, the particular row and memory bank are selected in response to the current access address), however, Lee does not specifically disclose a coherency engine.

However, it is well known in the cache art to using a coherency engine for the purpose of maintaining data consistency thereby increasing the memory access speed. For example, Handy discloses a coherency engine (Page 159).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to add a coherency engine of Handy into the invention of Lee for the advantages stated above.

As to claim 10, Lee and Handy disclose the invention as claimed in the above. Lee further discloses wherein said transaction request is a read transaction request (col. 5 line 51).

As to claim 11, Lee and Handy disclose the invention as claimed in the above. Lee further discloses transmitting data for said read transaction request from said one of said plurality of sub-unit caches to one of said plurality of client ports (col. 10 lines 23-28, the particular row and memory bank are selected in response to the current access address).

As to claim 12, Lee and Handy disclose the invention as claimed in the above. Lee further discloses prefetching one or more cache lines ahead of said read transaction request (cache memory reads on this limitation since the cache memory is used to assure that the currently useful data of main memory are copied into the small and fast cache for the purpose of increasing data access speed by means of spatial and temporal localities); and updating the coherency state (Sec. 4.3.1) information in said plurality of sub-unit caches.

As to claim 13, Lee and Handy disclose the invention as claimed above. Handy further disclose wherein said coherency logic protocol includes a Modified-Exclusive-Shared-Invalid (MESI) cache coherency protocol (Page 159).

As to claim 14, Lee and Handy discloses the invention as claimed in the above. Lee further discloses wherein said transaction request is a write transaction request (col. 5 line 51).

As to claim 15, Lee and Handy disclose the invention as claimed in the above. Handy further discloses modifying coherency state information for a cache line in said one of said plurality of sub-unit caches; updating coherency state information in others of said plurality of sub-unit caches by said coherency engine; and transmitting data for said write transaction request from said one of said plurality of sub-unit caches to memory (MESI protocol reads on this limitation and pages 159-161).

9. Claims 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. (Lee) U.S. Patent 6,477,621 in view of Jim Handy, "The Cache Memory Handbook" TK7895.M4H35, 1993, pp 140-240 and further in view of Witt et al. (Witt) U.S. Patent 6,202,139.

As to claim 16, Lee further discloses modifying coherency state information of said write transaction request (block 47), however, neither Lee nor Handy specifically discloses write transaction request in the order received and pipelining multiple write requests.

Witt discloses write transaction request in the order received and pipelining multiple write requests (col. 2 lines 42-43) for the purpose of avoiding bank conflicts

thereby decreasing the performance losses and increasing the access speed (col. 2 lines 43-45).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate write transaction request in the order received and pipelining multiple write requests as shown in Witt into the combined invention of Lee and Handy because it would avoid bank conflicts thereby decreasing the performance losses and increasing the access speed.

As to claim 17, Lee, Handy and Witt disclose the invention as claimed in the above. Handy further discloses wherein the coherency state information includes a Modified-Exclusive-Shared-Invalid (MESI) cache coherency protocol (Page 159).

Response to Arguments

10. Applicant's arguments with respect to claims 1-17 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See attached PTO-892.

2. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the

period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

3. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. ' 1.111(c).

4. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hong Kim whose telephone number is (571) 272-4181. The examiner can normally be reached on M-F 9:00 to 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 whose telephone number is (571) 272-2100.

6. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

7. **Any response to this action should be mailed to:**

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

or faxed to TC-2100:
(703) 872-9306

Hand-delivered responses should be brought to the Customer Service Window (Randolph Building, 401 Dulany Street, Alexandria, VA 22314).

H Kim
Primary Patent Examiner
April 14, 2005